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# SWITCHING AMPLIFIER DESIGN FOR MAGNETIC BEARINGS

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**Abstract**

Magnetic bearings incorporating linear feedback generally require an efficient transconductance power amplifier having a fairly broad bandwidth. The design evolution of an asynchronous switching amplification scheme which employs a novel control algorithm is presented. This design yields low harmonic distortion, excellent stability, good immunity to short-pulse failure and high efficiency.

In conjunction with the need for true transconductance behavior, the highly inductive loads inherent in magnetic bearing applications impose specialized demands which are not well met by conventional amplifiers. Adequate force slew rate requires large power supply voltage overhead which produces prohibitively low efficiency in linear (non-switching) amplifiers. Further, the variable nature of the load impedence renders precompensated open-loop schemes unsuitable.

These difficulties can be overcome by using a switching amplifier in a high gain current feedback loop. The high loop gain required to minimize error and provide wide bandwidth precludes the use of pulse width modulation (PWM) suggesting, instead, simpler bang-bang approaches.

Both hysteresis and sample-hold configurations were investigated and found to have significant shortcomings in this application. In particular, hysteresis amplifiers suffer from short-pulse susceptibility leading to low efficiency or output device failure. The sample-hold scheme provides excellent short-pulse immunity but produces fairly severe harmonic distortion, especially at low signal amplitudes.

A novel control algorithm, designated Minimum Pulse Width (MPW), is proposed. This approach is asynchronous as in the case of hysteretic control, yet imposes a restriction on the minimum pulse width delivered to the output devices. The resulting performance combines the low distortion of a hysteresis amplifier and the short-pulse immunity of sample-hold schemes. Experimental results are presented to support this claim.

## Introduction

Active magnetic bearings generate a force on the supported structure which is generally modeled as functionally related to the electric current in the electromagnet coils. In class A applications, opposing electromagnets are prebiased (either with a bias current or with permanent magnets) and the force generated is essentially proportional to a perturbation current applied to both opposing magnets [1-4]. In class B operation, only one of an opposing pair of magnets is activated at a time and the force is related to the square of the current [2]. The underlying assumption in control schemes developed for either of these two modes of operation is that the current in the electromagnet coils of the bearing can be controlled explicitly. Such control defines the operation of a transconductance power amplifier: the amplifier drives a current through a load which is proportional (over the bandwidth) to a command signal. Since the command signal is typically a voltage, the amplifier generates a current which is proportional to an applied voltage, hence the term transconductance.

Design of such an amplifier poses several interesting challenges. Traditional power amplifiers are usually not well suited for this application, as they typically provide an output *voltage* proportional to an input voltage. If the impedence presented by the magnetic bearing coils were fixed, then some sort of precompensation might permit true transconductance behavior over some bandwidth. Generally, the impedance of a magnetic bearing coil is a strong function of the operating conditions, rendering precompensation ineffective. For this reason, true transconductance behavior can only be achieved through a high gain current feedback loop around the load.

In addition to the need for explicit transconductance behavior, amplifiers used in magnetic bearing applications must posess sufficient voltage overhead to provide adequate current slewing (and thus bearing force slewing) capability. Given a particular force slew rate requirement for a bearing, the necessary supply voltage can be calulated from the nominal coil inductance and actuator gain [5]. The required supply voltage will typically be well in excess of the voltage needed merely to provide the coil bias current.

Early amplifier design at the University of Virginia involved the design and construction of a linear transconductance amplifier (see figure 1 for a simplified schematic of the output stage). This amplifier was designed to operate small experimental test rigs one of which exhibited $L_{coil} \approx 150$ mH (at nominal gap) and $R_{coil} \approx 20\ \Omega$. This rig is typically operated with bias currents of $\approx 500$ mA from a supply voltage of 100 VDC. Under these conditions, approximately 10 VDC appears across the coil, and roughly 90 VDC across the output MOSFET (leading to coil and amplifier dissipations of 5 and 45 W, respectively). Using the typical actuator gain for this rig ($\approx$ 125 lbf/A) and the calculated maximum current slew rate (667 A/sec) yields an approximate force slew rate limit of $\approx$ 83,000 lbf/sec. Subsequent bearing designs have been revised to bring the coil inductance into the 1-15 mH range and the coil resistance down to 1-10 Ω, thus permitting the use of higher current, lower voltage amplifiers to achieve the same force slew rates [6].

The principal drawback of linear amplifiers is that they are very inefficient, a characteristic further exacerbated by the high voltage overhead requirements imposed by magnetic bearing applications. The linear amp discussed above, for example, operates at approximately 10% efficiency and

dissipates roughly 450 W (45W × 10 channels) while operating a fairly small experimental rig. Clearly, such losses would be intolerable in higher power applications. For this reason, and because linear amplifiers must be tuned to the specific load to ensure stability of the current feedback loop, it was concluded that switching amplifiers might provide a better approach.

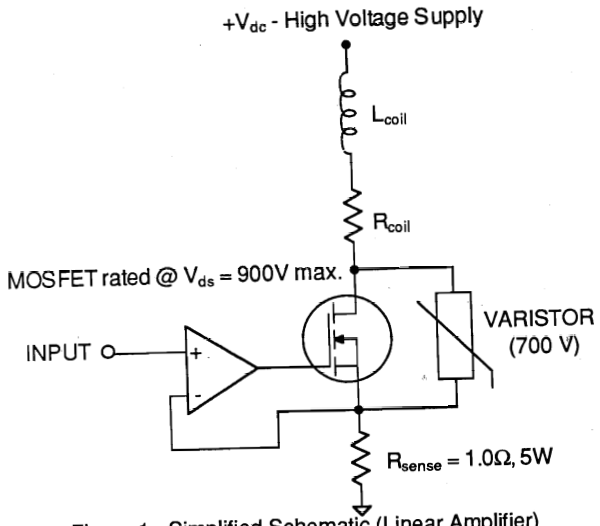


Figure 1 - Simplified Schematic (Linear Amplifier)

**Switching Amplifiers - General Characteristics**

Switching power amplifiers are distinguished from the more conventional linear power amplifiers in that the output voltage, rather than being continuously variable over some wide range, is restricted to two fixed levels. The purpose of this restriction is to minimize power losses in the output devices, which are generally some kind of transistor. Linear amplifiers, on the other hand, achieve a variable output voltage by controlling the resistance of the output transistors which are in series with the load between a fixed power supply and ground. Thus, at any output voltage intermediate between the power supply voltage and ground, the output transistors must dissipate power resistively.

Switching power amplifiers avoid this power dissipation by only operating the output transistors in a saturated "on" (low resistance) state or an "off" (very high resistance) state. Power dissipation in these amplifiers occurs primarily while the transistors are switching from one state to the other, with some power also being dissipated in the "on" state due to the non-zero on-resistance of the transistors. Because most of the power dissipation in these amplifiers occurs during the state transitions, the efficiency relies on keeping the switching rate below some threshold which depends upon the switching characteristics of the output transistors.

By switching the output stage at rates in excess of the required amplifier bandwidth (typical switching rates are 10-100 kHz) and varying the duty cycle of the output waveform, it is possible to create an output signal which combines the desired low frequency component with a higher frequency noise component. The nonlinear compensator in figure 2 regulates this switching; the form of compensation greatly effects the performance of the overall circuit. For example, a direct connection between the error amplifier and the output stage (i.e., the nonlinear compensator is a straight wire) results in a linear amplifier since the error signal will force the output devices to operate in their linear operating region. To achieve the efficiency potential of switching amplifiers, the nonlinear compensator must *restrict* the rate at which the output devices switch. Although the noise output components move to higher frequency bands as the switching rate of the amplifier is increased, this action progressively degrades its efficiency (in the limit, as the switching rate approaches infinity, the efficiency converges to that of a linear amplifier, since attempts at rapid switching yield operation in the linear region). Lower switching rates, while introducing more low frequency noise, generally dissipate less heat and result in more efficient operation. While switching amplifiers generally radiate significantly higher levels of EMI/RFI emissions than equivalently rated linear amplifiers, their efficiency can easily be an order of magnitude greater. The central design issue for a switching transconductance amplifier then becomes: given the requirements imposed above (load insensitivity, explicit control of coil current, efficiency, etc.), how does one determine the manner in which the output stage should be switched to achieve robust, high bandwidth, low distortion operation?

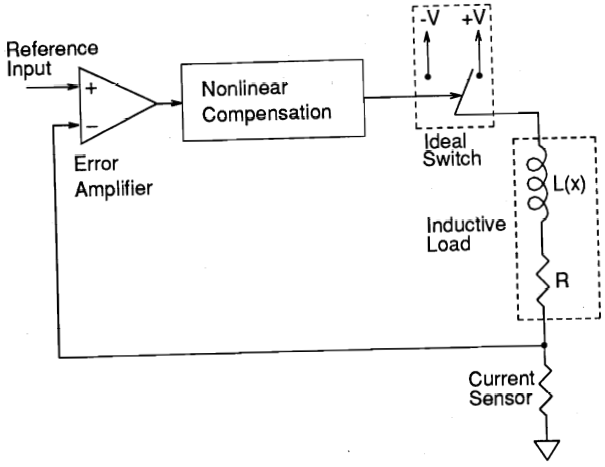


Figure 2 - Block Diagram of Generic Closed-Loop Transconductance Amplifier

The most widely used switching power amplifier is the Pulse Width Modulated, or PWM, amplifier. This amplifier is a voltage-to-voltage amplifier, generally employing no feedback. The linearization scheme employed in PWM amplifiers is to rapidly switch the voltage applied to the load between two fixed levels, $V_1$ and $V_2$, in such a way that the average voltage across the load is equal to the desired voltage. This is usually accomplished by comparing the input voltage to a high frequency triangle wave of fixed amplitude and frequency. As long as the reference triangle wave is smaller than the input voltage, the output devices are switched to apply $V_1$ ($V_1 > V_2$) to the load. When the reference triangle wave rises above the input voltage, the output devices are switched to apply $V_2$ to the load. In this manner, the duty cycle of the output pulse train is modulated to provide an average output voltage proportional to the command signal. All subsequent references to "PWM amplifiers" in this

paper are to the type of PWM amplifier described in this paragraph.

One common approach to the transconductance design problem is to precompensate a traditional PWM power amplifier so that the output current is proportional to the input voltage over some range of frequencies [7]. Such a configuration, shown in figure 3, has the advantage that its primary component, the PWM power amplifier, is readily available in the commercial market, and often includes the necessary precompensation circuitry [8]. However, the precompensation circuit in the open-loop PWM solution must be tuned to the load impedence - a troubling constraint, given that the coil characteristics of magnetic bearings are typically ill-defined and when, in addition, the coil impedence changes with the gap between the magnetic bearing pole pieces and rotor laminations.

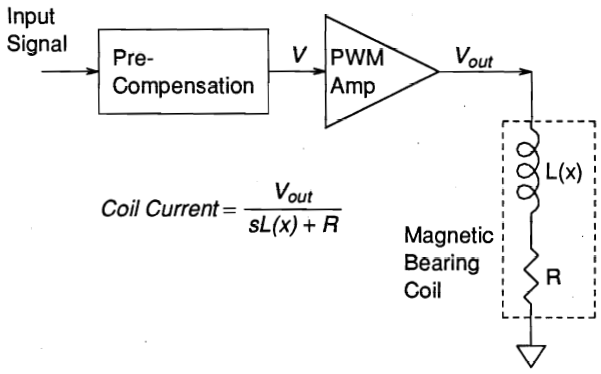


Figure 3 - Open-Loop PWM Transconductance Amplifier

The same PWM amplifier can be used to produce a transconductance amplifier in the configuration of figure 2. However, this scheme still has a number of drawbacks. Operation of a PWM amplifier in its continuous region imposes restrictions on the maximum voltage slew rate that can be applied to its input (see figure 4). This, in turn, restricts the amount of gain which can be employed in the feedback loop, which reduces both the low frequency accuracy and bandwidth of the amplifier. Increasing the error amplifier gain (or increasing the gain of the *linear* compensation block in figure 4) can reduce this error, but such action tends to present large, rapidly-changing voltages to the PWM generator. These input voltages will tend to saturate the PWM amplifier at either zero percent duty cycle (off) or 100 percent duty cycle (on) during each period of the PWM reference triangle wave. As the gain of the error amplifier is made large, the PWM amplifier begins to operate as a simple sample and hold device: it ceases to switch during its sampling interval, remaining either "on" or "off" for each entire interval.

**Bang-Bang Algorithms - Sample/Hold and Hysteresis**

This sample and hold behavior is not necessarily undesirable, but it can be accomplished with far simpler circuitry than that of a PWM amplifier. A simpler approach to building a switching transconductance amplifier for driving inductive loads is a "bang-bang" control system with a fixed sampling rate [9, 10]. This scheme involves driving the output transistors directly with the current comparator signal: when the output current is larger than the requested current,

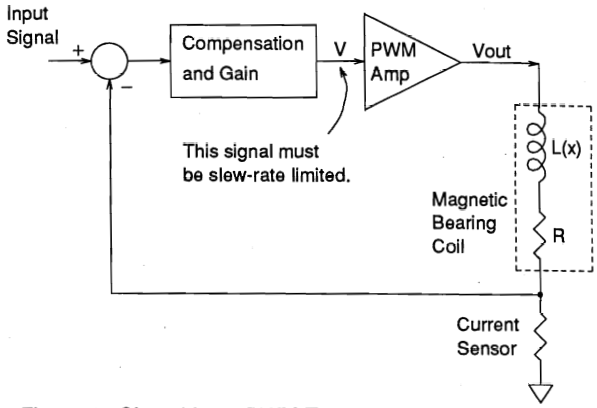


Figure 4 - Closed-Loop PWM Transconductance Amplifier

the output transistors switch the output voltage to its "low" value; when the output current is smaller than the requested current, the output transistors switch the output voltage to its "high" value. In order to restrict the switching to a rate which provides high efficiency, a sample-and-hold device is inserted between the comparator and the output stage. This device is driven by a periodic clock. At the beginning of each clock period, the sample-and-hold device transfers the state of the comparator to the output devices. This state is then retained for the remainder of the clock period. In this manner, the maximum switching rate is fixed by the clock (see figure 5). The *D flip-flop* shown in figure 5 is logic circuit which performs the sample/hold action on discrete binary signals.

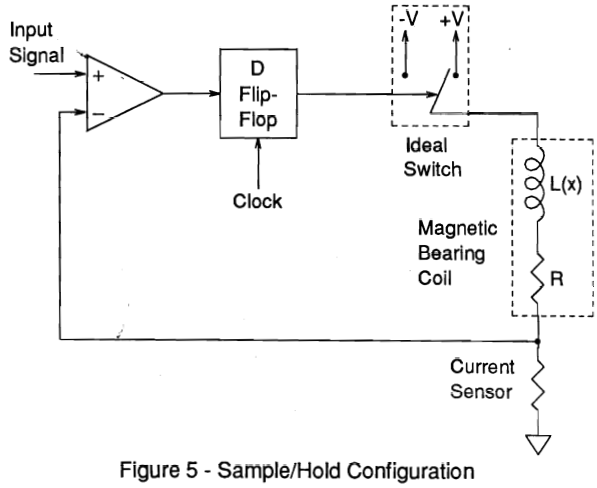


Figure 5 - Sample/Hold Configuration

Fixed sampling rate control can be implemented with a fairly simple circuit, giving it a substantial advantage over PWM control. Its primary drawback is that, because the switching instants are fixed by the clock, it tends to produce significant harmonic distortion. It also exhibits a deadband rendering it very insensitive to small signals.

Figure 6 presents simulated and measured time response data for the sample/hold configuration. The simulated data was generated by digital computer with idealized models for the comparator, current sensing, output switch, and series inductive/resitive load. The measured response was captured

with a digital storage oscilloscope.

Casual inspection of figure 6 reveals discrepancies between the simulated and measured responses. These differences result from characteristics of the experimental setup which remain unmodelled in the simulation: nonidealities of the output devices driving the load, and asymmetric propagation delays generated by the control circuitry in the power output modules [11]. The simulation program models the IGBT output devices used for these experiments as ideal switches, a model which ignores the static voltage drop and poor high frequency dynamic performance of the transistors (for example, the manufacturer of the devices used here recommends that they be switched no faster than 20 kHz; our sample/hold controller switches at 62.5 kHz). The greatest contributor to the discrepancy, however, is the asymmetric propagation delay between control pulse and output device response. Close inspection of the sample/hold waveform reveals that, while the *average* sample period is 16 μS (as it should be), the amplifier often generates successive pulses of, for example, 13 μS and 19 μS. Such behavior, not accounted for in the simulation, significantly alters the operating characteristics of the sample/hold amplifier. This behavior, though, is uniquely a function of the particular output modules employed here and is not intrinsic to the sample/hold algorithm. In any event, both the simulated and measured responses display the substantial distortion typical of sample/hold operation.

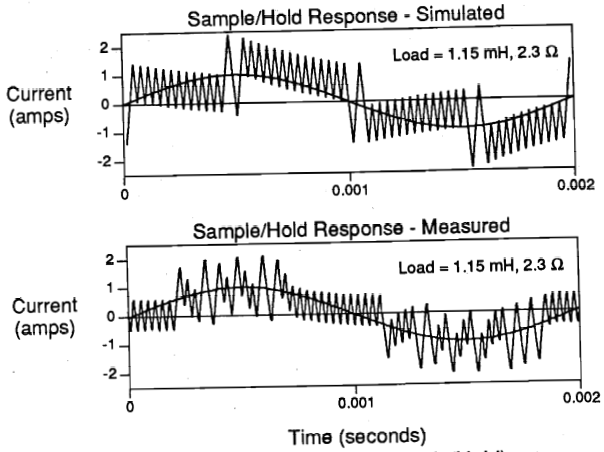


Figure 6 - Time Responses (Sample/Hold)

The decision-making capability of the sample/hold amplifier can be significantly improved if these decisions are allowed to occur in an asychronous manner. Rather than fixing each switching instant with an impartial clock, the load response should determine each switching instant directly. At the same time, the switching rate needs to remain restricted. One method of achieving such behavior is to add a small amount of hysteresis to the comparator so that rather than switching to a positive state precisely when the current error becomes positive and switching to a negative state precisely when the error becomes negative, the positive transition is delayed until the error reaches some threshold value, $+\varepsilon$, and the negative transition is delayed until the error reaches another threshold, $-\varepsilon$. When the amplifier is driving an inductive load, these voltage thresholds yield a time delay due to the integrating effect of the load. Thus, a fixed period sample/hold device is apparently not required to control the maximum switching rate: the output of the hysteretic comparator can drive the output devices directly with no intervening logic.

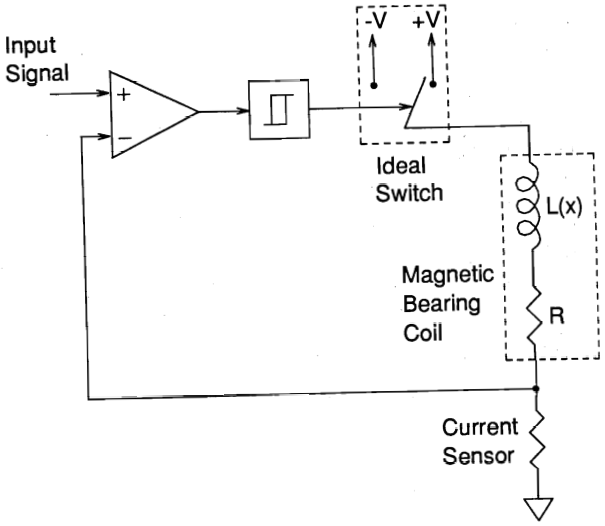


Figure 7 - Hysteresis Configuration

The circuit required to implement hysteretic control is even simpler than that required for fixed sampling rate control, dispensing with the clock and the sample-and-hold device at the expense of only a few resistors needed to produce the desired hysteresis. The absence of a fixed sampling rate results in an asychronous configuration which exhibits greatly reduced harmonic and crossover distortion (note the tight tracking and low distortion of the simulated response in figure 8). The most apparent drawback to this design is that the switching rate will depend not only on the amount of hysteresis designed into the circuit, but also on the load impedance and the power supply voltages. Consequently, the amplifier must, to some extent, be tuned to the load in order to ensure that the switching rate does not exceed the maximum allowed by the output stage while remaining high enough to yield good bandwidth. A more insidious problem inherent in hysteretic control is that it can produce very short control pulses if the reference signal changes rapidly [12]. This is particularly a problem in the presence of noise in the reference signal. In the simple analysis, short control pulses will only seem to degrade the efficiency of the amplifier, but if the output stage is an H-bridge, short pulses may cause device failure. (Some commercial H-bridge power devices have short pulse detection circuits to avoid this: short pulses will cause the output device to turn off [11].)

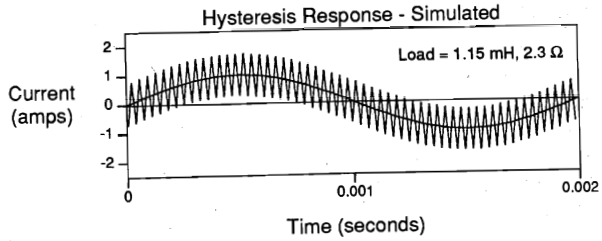


Figure 8 - Time Response (Hysteresis)

It is instructive to compare the distortion characteristics of the sample/hold and hysteresis amplifiers. Figures 9 and 10 show simulated waveform reconstructions obtained by performing a Fourier analysis over 20 cycles of amplifier response to a sine wave excitation and then summing the first 12 harmonics. The resulting waveforms confirm what might be expected from inspection of the time response plots: namely, that the hysteresis algorithm introduces much less distortion than the sample/hold approach does. These results also illustrate that, as the amplitude of the reference input signal is reduced, the distortion characteristics of *both* types of amplifier grow worse. However, even for the 1 amp experiment (figure 10), the hysteresis amplifier generates less than 1 percent THD, and the reconstructed waveform is virtually indistinguishable from the reference input. (It should be pointed out that, all else being equal, increasing the load inductance will improve the distortion characteristics of any of these control schemes). Clearly, an algorithm which embodies the distortion characteristics of the hysteresis approach yet does not demonstrate its shortcomings offers significant improvements over the sample/hold design.

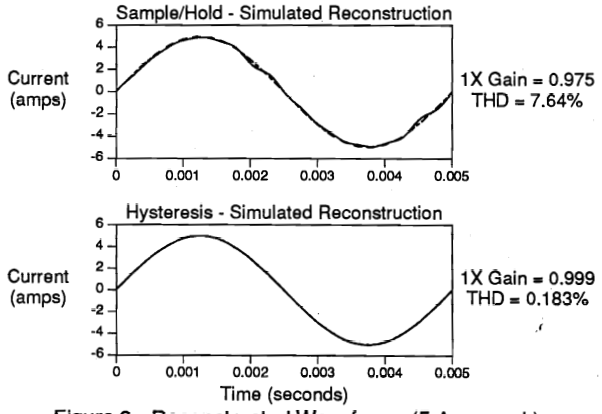


Figure 9 - Reconstructed Waveforms (5 Amp peak)

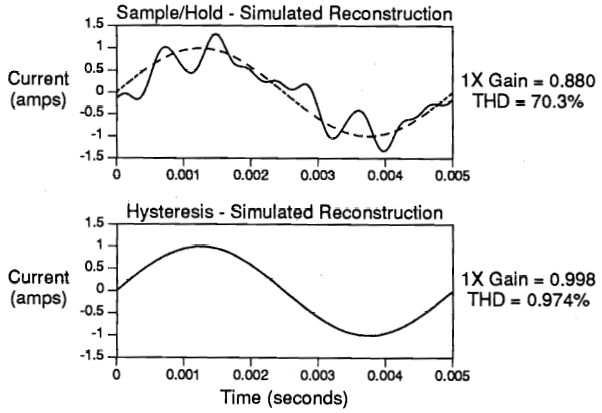


Figure 10 - Reconstructed Waveforms (1 Amp peak)

### Minimum Pulse Width Configuration

The Minimum Pulse Width power amplifier, hereafter referred to as the MPW amplifier, is intended to achieve the high efficiency of a switching amplifier without some of the drawbacks of prior designs such as high complexity, high distortion and short pulse fault susceptibility.

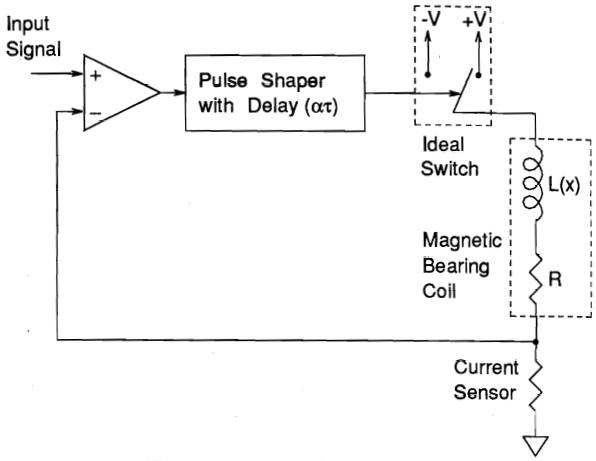


Figure 11 - MPW Configuration

The primary shortcoming of hysteresis control is its short pulse susceptibility. One solution to this problem is to insert a pulse shaping circuit after the hysteresis element which either strips short pulses out of the pulse train or stretches them to an acceptable length. While this would eliminate the short pulse problem, it suggests a further simplification. Since the primary objective of the hysteresis is to produce finite length pulse, but the same function is also provided by the pulse shaping circuit, the hysteresis is now unnecessary. These considerations lead directly to the design of the minimum pulse width amplifier.

The MPW amplifier is constructed in the same basic configuration as the previously mentioned sample/hold and hysteresis schemes (see figure 11). However, the nonlinear compensator consists of simple digital logic which keeps the pulse width of the control signal applied to the output device greater than some fixed minimum. The operation of this pulse shaper can be summarized as follows. Each incoming pulse is delayed by a period of $\alpha\tau$ where $\alpha$ is a fixed number ranging between zero and one while $\tau$ is the minimum permissible pulse width. At the end of the time delay interval, if the pulse shaper detects that the incoming pulse has ended (the incoming pulse width was less than $\alpha\tau$) then the pulse is not transmitted. Thus, pulses of duration less than $\alpha\tau$ are stripped from the pulse train. On the other hand, if the pulse has not ended prior to $\alpha\tau$, it is transmitted to the output of the pulse shaper and the output state is retained for a duration of at least $\tau$. In this manner, pulses of duration greater than $\tau$ are delayed by a period $\alpha\tau$, but otherwise are not modified. Pulses of duration less than $\tau$ but greater than $\alpha\tau$ are also delayed by $\alpha\tau$ but, in addition, are extended to a duration of $\tau$. This behavior is summarized in figure 12.

The primary differences between this design and the previous techniques are:

1.) in a fixed sampling rate controller, switching can only occur at the clock edge; with MPW, the transition can occur anytime up to within the minimum pulse period of the last transition.
2.) in a fixed sampling rate controller, the control pulse period must be an integer multiple of the clock period; MPW permits control pulse periods to vary continuously

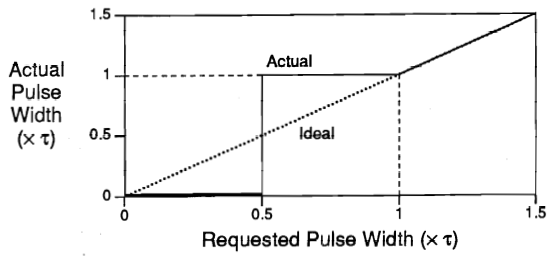


Figure 12 - Pulse Width Transfer Function ($\alpha = 0.5$)

from the fixed minimum period to infinity.

3.) in a fixed sampling rate controller, control pulses emanating from the comparator are always extended to the nearest integer multiple of the clock period; MPW extends only those pulses which are between one half the fixed minimum pulse width and equal to the fixed minimum (shorter pulses are discarded and longer pulses are not altered).

4.) fixed sampling rate control does not explicitly introduce a time delay between the control pulse emanating from the comparator and that delivered to the output device, but a time delay is implicit since this control scheme always extends the preceding pulse; MPW introduces a fixed time delay equal to one half the minimum pulse width ($\alpha = 0.5$).

5.) hysteretic control does not explicitly restrict the minimum pulse width seen by the output devices; this restriction is one of the motivating characteristics of MPW control.

6.) the switching times in a fixed sampling rate controller are determined by a regular clock (i.e., a synchronous configuration); the MPW configuration has no clock and operates aynchronously.

The objective in stripping off short pulses rather than extending them to the minimum pulse width is to eliminate a small signal deadband which results from always extending them (see figure 13 for simulated time responses which show the effect of increasing the "strip off" threshold from 0 to $0.5\tau$, where $\tau$ is the minimum pulse width allowed). Short pulse detection cannot be accomplished without observing the first $\alpha\tau$ portion of the pulse. This necessarily implies a time delay of $\alpha\tau$; however, choosing $\alpha = 0.5$ eliminates the deadband and minimizes harmonic and crossover distortion. It is important to realize that there is no advantage to increasing $\alpha$ beyond $0.5\tau$; in fact, such action merely reduces the bandwidth of the amplifier (by increasing the delay in the feedback loop) and moderately increases the THD seen in the output signal (see figures 14 and 15 for plots of typical 1X (fundamental) gain and THD versus $\alpha$). Introduction of the $\alpha$ delay in the feedback loop has the additional effect of increasing the amplitude of the output switching noise, which is the predominant reason for the increased THD beyond $\alpha = 0.5$ (this increase in output noise is evident in the plots of figure 13).

Figure 16 shows the simulated and measured waveforms for the MPW amplifier. Note that the agreement between simulation and measurement is much better than in the case of the sample and hold scheme. This reflects the fact that the asynchronous nature of the MPW control scheme renders it much less sensitive to the asymmetric propagation

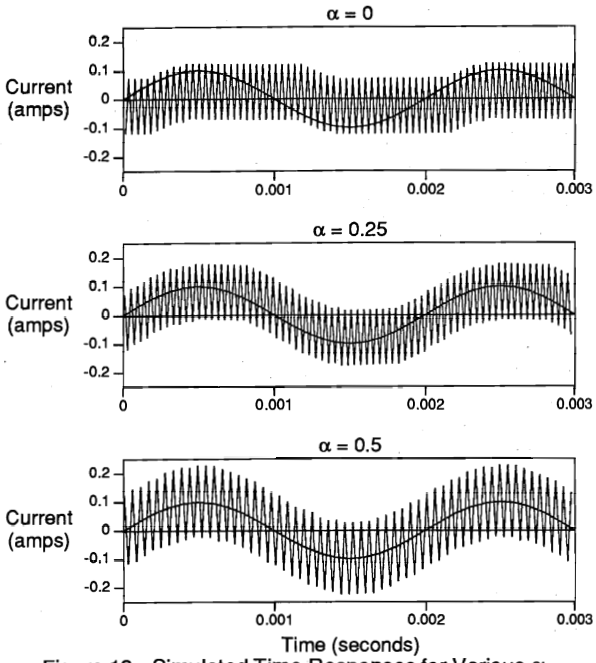


Figure 13 - Simulated Time Responses for Various $\alpha$

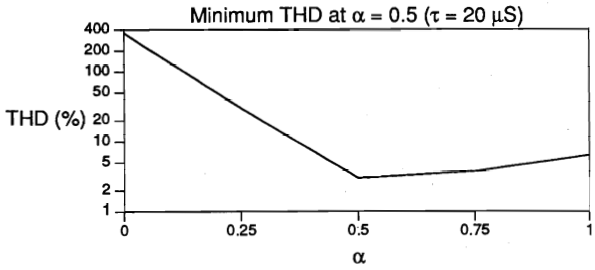


Figure 14 - Total Harmonic Distortion versus $\alpha$

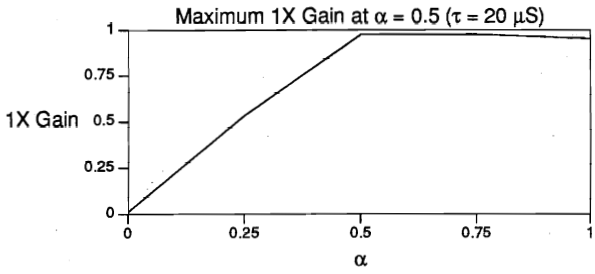


Figure 15 - Fundamental Gain versus $\alpha$

delay in the output devices.

The MPW time response of figure 16 can be compared to the hysteresis time response shown in figure 17, where the hysteresis level has been adjusted to give approximately the same noise level in the two waveforms. The excellent agreement between these traces supports the argument that the MPW configuration provides most of the advantages of hysteresis control. This agreement is even more evident in comparing the filtered responses shown in figures 18 and 19. As before, the simulated waveforms are reconstructed by adding

the first twelve harmonic responses as determined by Fourier analysis. This removes the switching noise while retaining the most significant distortion characteristics. The similarity of the fine structure in figure 19 is particularly striking.

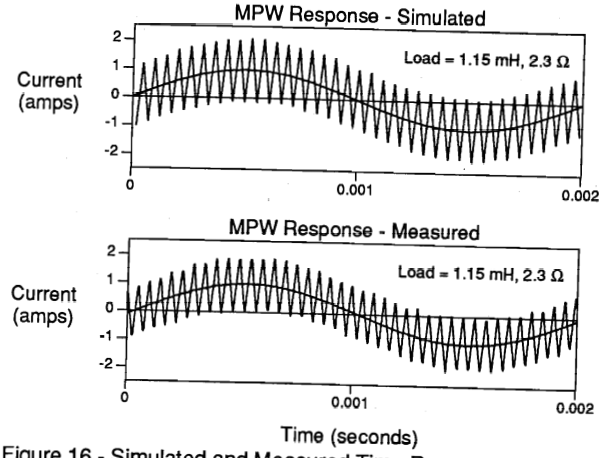


Figure 16 - Simulated and Measured Time Responses (MPW)

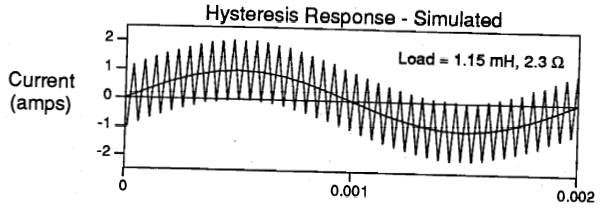


Figure 17 - Simulated Time Response (Hysteresis)

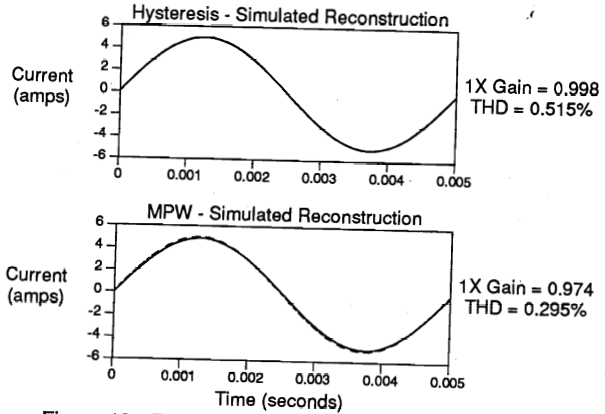


Figure 18 - Reconstructed Waveforms (5 Amp peak)

## Additional Experimental Results

With any amplifier, especially one destined for application in a closed-loop control system, the frequency response is a performance index of interest. Figure 20 shows responses for the MPW amplifier under the following conditions: 100 mV, 2 V or 8 V (peak) sine wave input, swept from 100 Hz to 25.6 kHz; 1.15 mH, 2.3 Ω load; $V_{supply}$ = 100 VDC; amplifier gain is 1 A/V. Note that the effective bandwidth of the amplifier depends on the excitation amplitude: as this value is increased from 2 V to 8 V (peak), the

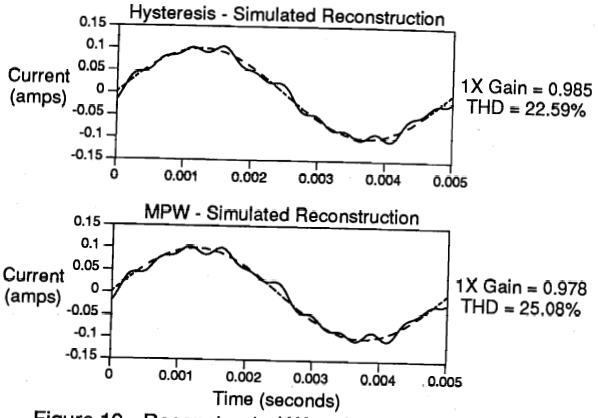


Figure 19 - Reconstructed Waveforms (100 mA peak)

"break point" in the response curve is reduced from approximately 7 kHz to about 1.8 kHz. This amplitude dependence is characteristic of systems experiencing nonlinear limiting; here, operation of the amplifier beyond the break point incurs transconductance errors as the slew rate limits of this particular supply voltage/load inductance combination are exceeded. Slew rate limiting is discussed extensively in [4], [5] and [13].

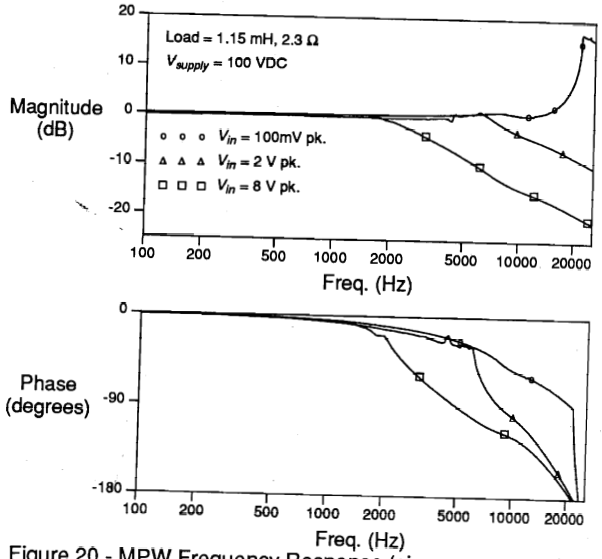


Figure 20 - MPW Frequency Response (sine wave sweep)

Two additional properties of the MPW amplifier should be noted. First, it is important to realize that the break point in the frequency response curve is *not* the same as the "-3 dB" point often referred to in linear system analysis (note that the phase response of the MPW amplifier is not -45 degrees at the break point as would be expected for a linear system). Also, significant aliasing is observed for the low amplitude curve at frequencies higher than ≈ 20 kHz (this behavior is manifested as an apparent increase in gain for these frequencies). Since this amplifier is a sampled-data system, Shannon's sampling theorem [14, 15] states that operation above the Nyquist frequency (defined as 0.5 × sampling rate) will result in aliasing. With a minimum pulse width of 23

μS, the effective maximum switching rate of this MPW amplifier is ≈ 44 kHz, which implies a Nyquist frequency of ≈ 22 kHz. Typically, devices of this sort are considered to have usable bandwidths no wider than one half of the Nyquist frequency.

## Conclusions

The results presented in this paper successfully establish the viability of a new type of switching transconductance amplifier, the Minimum Pulse Width amplifier. These results demonstrate attainment of the stated design goal of low harmonic distortion, and by design the MPW amplifier is fundamentally immune to short-pulse failure. With no particular precautions or tuning performed, an amplifier of this design has been operated successfully with loads varying from 1-200 mH, thus demonstrating its insensitivity to load variations.

Earlier approaches to the transconductance amplifier design problem were investigated. Open-loop schemes employing conventional PWM voltage-to-voltage amplifiers exhibited a high degree of sensitivity to the load impedence and required tuning to achieve transconductance behavior. Introducing current feedback around such a PWM amplifier reduced this load sensitivity, but the closed-loop configuration was still unnecessarily complex and suffered from low frequency accuracy and bandwidth limitation problems.

Two bang-bang control schemes (sample/hold and hysteresis) were considered. Both of these configurations overcame the complexity problems associated with conventional PWM amplifiers, but each presented different limitations. The sample/hold design produced significant harmonic distortion and exhibited a deadband which rendered it insensitive to small signals. The hysteresis demonstrated very low distortion behavior, but suffered from short-pulse susceptibility which could potentially degrade efficiency and destroy output devices during normal operation.

The Minimum Pulse Width (MPW) design was presented. Simulated and measured results from the MPW amplifier confirm that it overcomes both the harmonic distortion problem of the sample/hold approach and the short-pulse susceptibility problem of the hysteresis configuration. Measured frequency response data for the MPW amplifier was presented; this data demonstrated the amplitude dependence expected for a system experiencing slew rate limiting and the aliasing characteristic of sampled-data systems operated above their Nyquist frequency.

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