FPGA-Based Implementation for Unbalance Compensation in Active Magnetic Bearings

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Abstract: An FPGA implementation for unbalance compensation in AMB is proposed. The compensation method uses a generalized notch filter based on coordinate transformations. In the FPGA implementation, the lookup table is used to get the sine and cosine value, and an incremental algorithm is adopted when calculating $\sin \Omega t$. The rotation speed of the flywheel rotor is considered as a constant in every iterative step. Detailed skills in HDL coding are presented. Experimental results prove that the compensation is effective over a wide range of operation speeds.

Keywords: Active Magnetic Bearings, Unbalance Compensation, FPGA Implementation

Introduction

Unbalance effects are great concern in AMBs. When the rotor's geometric axis and mass axis are not one, the synchronous unbalance force will result in rotor runout, and consequently, reduction in rotational accuracy. Besides, rotor runout rises dramatically when the rotational speed is approaching critical frequency, in those cases the rotor may hit the retainer bearings [1].

The unbalance effect can be attenuated by canceling the synchronous unbalance component in signals from eddy current sensors. Many control strategies have been developed to do it [2]-[5]. In 1990 Matsumura *et al.* developed the unbalance disturbance rejection method based on the state feedback control approach [2]. Herzog *et al.* proposed a generalized notch filter in 1996 to figure out the stability problem caused by single insertion of notch filters in the control loop [3]. The generalized notch filter can deal with the synchronous signals at a wide range of rotation speed with the ability of free pole location. These methods have the drawback that the unbalance compensation controller alters the control loop's transfer function or sensitivity function, thus changes the system's performance. As a result, recent works focused on "add-on" controllers which can be designed independently as additional controller to generate the synchronous compensation signals. Based on frequency-domain iterative learning control, Knopse *et al.* proposed an adaptive vibration control method in which look-up tables were used to select a gain matrix according to operation conditions [4]. In 2005, Chao Bi *et al.* pointed out that most of the existing methods require the precise prior knowledge of AMB parameters, and, proposed the automatic learning control for unbalance compensation by improving the iterative learning control algorithm [5].

Most of the above methods can provide satisfying compensation effects, but many of them are too complicated to be implemented on some commercial-off-the-shelf (COTS) devices. Recently, the field programmable gate arrays (FPGA) were effectively used as a platform in the implementation of control systems and power amplifiers of AMB [6], [7]. It is shown that both the precision and the speed of the computation can meet the needs of the high-bandwidth systems with the help of floating-point operation IP cores [7]. In this paper, a scheme based on coordinate transformations is presented to generate the synchronous compensation signals which were added to the input of the control system of AMB to reject unbalance effects. An FPGA implementation is proposed. Some algorithm refinement is presented to make the application of the reuse methodology conveniently. Test results prove the effectiveness of the scheme and the implementation.

Problem definition of unbalance compensation for AMB

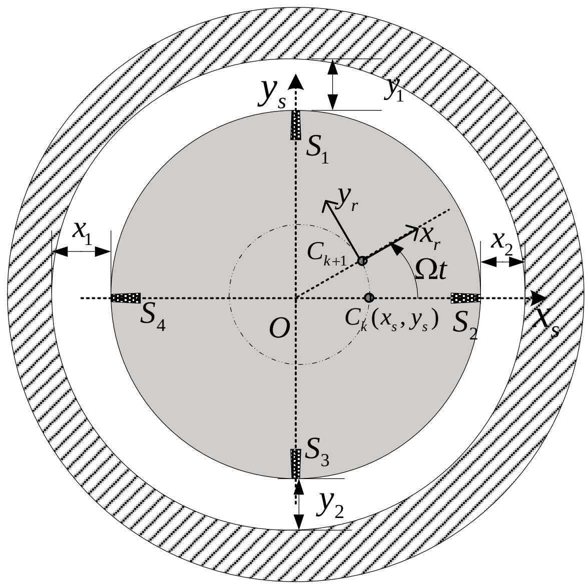


Figure 1 Definition of unbalance compensation in a 2-D plan outer rotor AMB

For a 2-D plan outer rotor AMB, as shown in Fig.1, if the four eddy current sensors $S_1 \sim S_4$ have no displacement in fixing, then in coordinate $X_s - O - Y_s$ the geometric center of the rotor could be defined as C, its coordinate is (x_s, y_s), $x_s = x_1 - x_2, y_s = y_2 - y_1$, if the rotor is perfectly round. Because of the unbalance effect, C will rotate around on O.

Unbalance compensation in AMB can be carried out in two ways: reduction of rotor runout and reduction of coil current fluctuations [5]. In this paper, the principle of unbalance compensation is to reduce the distance between C and O because in our application, a high level of rotational accuracy is required.

Unbalance compensation scheme based on coordinate transformation

The unbalance compensation scheme based on coordinate transformation shown in Fig.2 is adopted in this paper [8]. Details in the synchronous signals processing unit is shown in Fig.3.

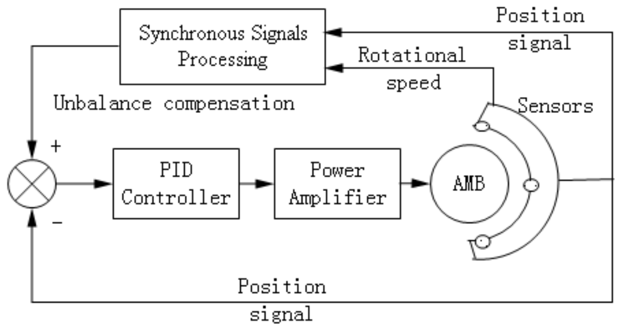


Figure 2 Scheme of unbalance compensation in a 2-D plan outer rotor AMB

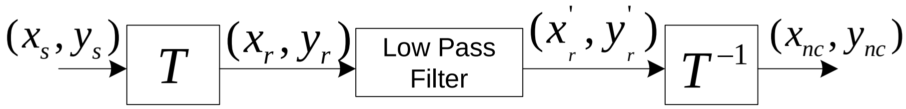


Figure 3 Synchronous signals processing unit in a 2-D plan outer rotor AMB

The steps of the synchronous signals processing are:

1) Use coordinate transformation T to get the position coordinate (x_r, y_r) of C in $X_r - C - Y_r$. Coordinate $X_r - C - Y_r$ is fixed with the rotor, rotating around O at the same speed with the rotor.

$$\begin{cases} x_r = x_s \cos \Omega t + y_s \sin \Omega t \\ y_r = -x_s \sin \Omega t + y_s \cos \Omega t \end{cases} \qquad (1)$$

2) Filter the position signals (x_r, y_r) with a low pass filter $G_{nf}(s)$.

$$G_{nf}(s) = \frac{1}{\frac{1}{2\pi f} \cdot s + 1}, \; f = 10 \sim 20Hz \qquad (2)$$

3) Transform the filtered position signals (x_r', y_r') back into $X_s - O - Y_s$ to get the unbalance compensation signals (x_{nc}, y_{nc})

$$\begin{cases} x_{nc} = x_r' \cos \Omega t - y_r' \sin \Omega t \\ y_{nc} = x_r' \sin \Omega t + y_r' \cos \Omega t \end{cases} \qquad (3)$$

Algorithm Refinement and FPGA Solution

In FPGA implementation, an incremental algorithm is adopted when calculating $\sin \Omega t$ and $\cos \Omega t$. The advantage of the incremental algorithm is that the calculation of sine and cosine can be done using only lookup table and MACs, which are common logic resources in FPGA. The lookup table in FPGA is generated by storing a series values of $\sin \Omega T$ and $\cos \Omega T$ at different rotational speed Ω. T is the sampling period for A/D conversion on the FPGA board.

$$\begin{cases} \sin(\Omega t + \Omega T) = \sin(\Omega t)\cos(\Omega T) + \cos(\Omega t)\sin(\Omega T) \\ \cos(\Omega t + \Omega T) = \cos(\Omega t)\cos(\Omega T) - \sin(\Omega t)\sin(\Omega T) \end{cases} \qquad (4)$$

As to the low pass filter, its z-domain transfer function (5) can be expressed as equation (6), which in turn, can be implemented using MACs as shown in Fig.4. Each block in Fig.4 is a floating-point V3.0 IP core provided by Xilinx Foundation ISE tools. The data structure of the signals and coefficients involved in these MAC operations complies with the IEEE-754 standard. The precision is 24 bits with 16-bit fraction and 8-bit exponent.

$$G(z) = \frac{y(z)}{u(z)} = \frac{a + bz^{-1}}{c + dz^{-1}} \quad (5)$$

$$y(k) = par1 \cdot u(k) + par2 \cdot u(k-1) + par3 \cdot y(k-1) \quad (6)$$

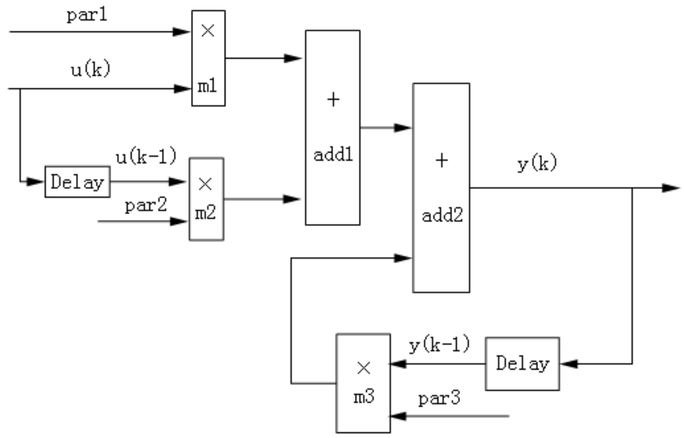


Figure 4 Block diagram of FPGA implementation for a low pass filter

Experimental Results

The FPGA board implementing unbalance compensation is shown in Fig.5. The performance of the board, namely, the compensation results, is shown in Fig.6 & Fig.7. Table 1 is a summary of the logic resources used in FPGA.

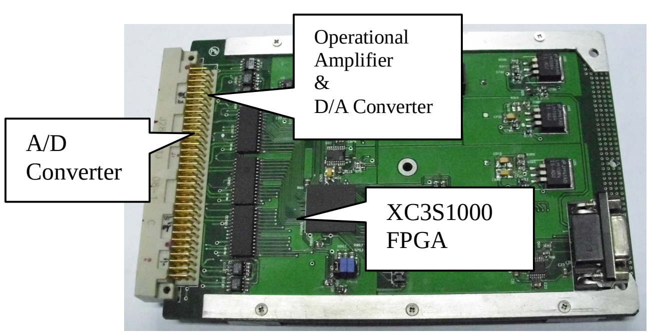
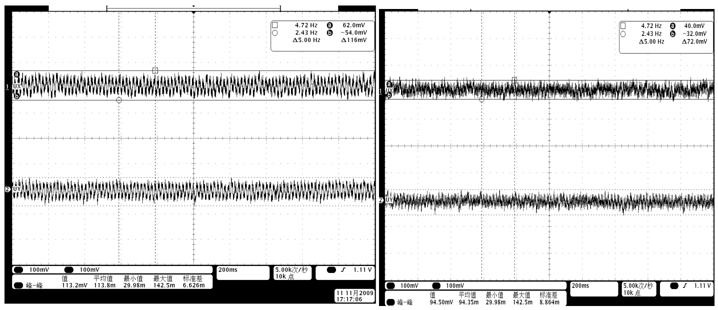
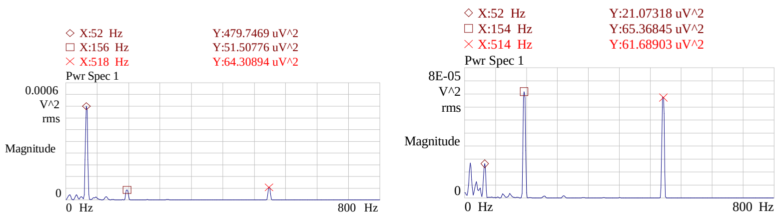


Figure 5 The FPGA board implementing unbalance compensation



(a) (b)

Figure 6 Performance of the FPGA board in time domain waveform. (a) Before unbalance compensation. (b) After unbalance compensation.



(a) (b)

Figure 7 Performance of the FPGA board in frequency spectrum. (a) Before unbalance compensation. (b) After unbalance compensation.

Table 1 Logic Resources Utilization

Target Device :	xc3s1000		
Number of Slice Flip Flops:	**5,183 out of**	**15,360**	**33%**
Number of 4 input LUTs:	**6,112 out of**	**15,360**	**39%**
Number of bonded IOBs:	**27 out of**	**173**	**15%**
Number of MULT18X18s:	**13 out of**	**24**	**54%**
Number of GCLKs:	**2 out of**	**8**	**25%**
Number of DCMs:	**1 out of**	**4**	**25%**
Total equivalent gate count for design:	**159,505**		

Conclusions

In this paper, a method based on coordinate transformations is adopted to generate the synchronous unbalance compensation signals. The compensation signals are added to the position signals of the AMB's rotor to reject the unbalance effect. In the FPGA implementation of the unbalance compensation, some algorithm refinements are made and a universal block based on floating-point operation IP cores is presented to capitalize the designing efforts. Test results demonstrate both the algorithm and the implementation are effective.

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