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HARDWARE PLATFORM FOR MAGNETIC BEARING CONTROL IN MACHINE-TOOL APPLICATIONS

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ABSTRACT

In this paper a new and powerful control hardware for magnetic spindle applications is presented.

The Hardware consists in two boards. The processor board assembles a floating point DSP, a high density FPGA and a TCP/IP communication Module. It is in charge of the control algorithms processing, system monitoring and real time data acquisition. The interface board assembles all the hardware modules needed to access external devices such as digital I/O, ADCs and DACs, encoder modules and so on. Moreover the most prominent features of the hardware devices and the reasons that have motivated the new design are described.

Since control strategy imposes computation requirements, a brief description of control algorithms is included. How this algorithm is distributed along the processor device is discussed as an example for control software implementation in the new hardware.

Finally, the new hardware design performance and benefits are enumerated and future work is presented.

INTRODUCTION

During the last two decades the technology based on active magnetic bearings has become an effective alternative to conventional bearings. It has also found industrial applications such as turbomolecular pumps and kinetic energy storage systems. The frictionless performance removes the use of lubrication and allows the system to work under hard conditions like high vacuum or high temperature environment. At the same time, the magnetic suspension provides long life and maintenance free systems, which must be taken into account in a high speed system due to the huge load that bearings support [1].

Therefore, magnetic bearings promise an ideal candidate for machine-tool applications, that is why a considerable effort is being made in this research area [2] [3]. The main issue to be solved is to deal with high requirements on positioning accuracy and performance robustness which impose an optimized mechanical and electromagnetic design and a complex control strategy.

In fact, magnetic bearings are inherent unstable so it is necessary to provide a controller that guarantees an adequate system behaviour. Taking advantage of this active controller, the system dynamic can be improved removing vibrations or non desirable dynamic due to shaft unbalance.

EXPERIMENTAL SYSTEM DESCRIPTION

Tekniker-IK4 has developed a magnetic spindle prototype that is nowadays working in a high speed milling machine.

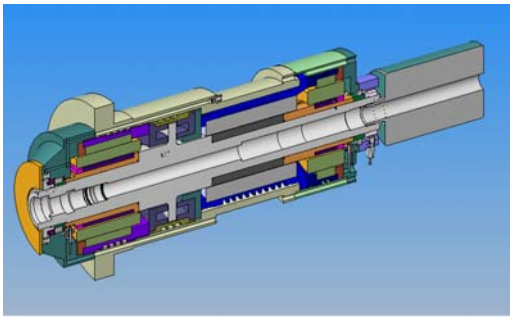

FIGURE 1: Magnetic bearing spindle for milling machine

The spindle has two eight-pole radial magnetic bearings and an axial one with 0.6 mm air gap. Current amplifiers provide up to 20 Amps to the bearing coils in

order to obtain 3200 N force. It uses 70 kw induction motor with a maximum speed of 36000 rpm

There are five sensors to measure displacements along the five degrees of freedom as well as temperature sensors to detect overtemperature in the bearings and the motor coils.

The prototype has been successfully tested working with aluminium parts, obtaining good accuracy and avoiding breakdown events when high load is applied to the tool.

CONTROL HARDWARE DESIGN CONSIDERATIONS.

Control algorithm

Due to the high position accuracy needed in machine-tool processes the main goal of the control is to achieve very high stiffness that guarantees a low response time and small displacements under machining forces. Good damping is also needed in order to mitigate either chatter, a harmful phenomenon for machining process, or undesired vibrations. The control is made using PIDs, so high stiffness is reached by designing a controller with proportional and derivative constants as high as possible. Nevertheless, increasing the value of those constants the system becomes unstable and tends to oscillate. In fact, one of the most important issues in system stability is to deal with the inherent noise in the position signals, so a complex filter line was included in the controller design containing antialiasing filters, lowpass filters and adaptive filters (Kalman filters) for each position sensor signal.

That controller was implemented using

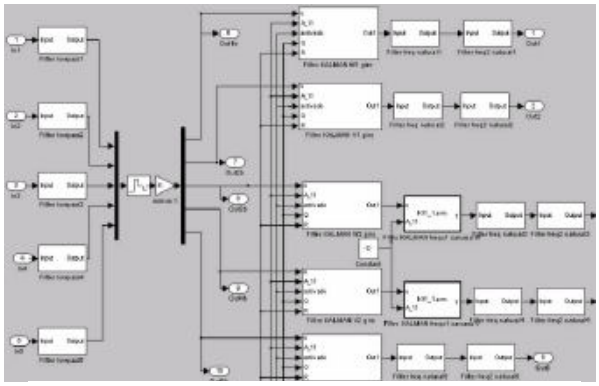

FIGURE 2: Matlab/Simulink Filter line block diagram.

Matlab/Simulink development environment to validate it in simulation tests. In the first experimental stages a PC system with acquisition board and I/O interface board was used as control hardware. Real-Time Workshop toolbox from Matlab/Simulink allows automatic translation of the control algorithms and the download of a Simulink-based model to the processor PC. By this, along with the real time operating system from Matlab, the processor PC has at its disposal all the resources to perform the control algorithm.

Experimental results confirm that the inclusion of the filter stages improves system behaviour, but such filter lines introduced another problem in the controller design. The computational cost increase considerably and the control loop frequency decrease. To guarantee a stable phase margin it is necessary to increase control loop frequency far from system bandwidth, which involves hard controller computation effort.

Although they are not yet implemented, active magnetic bearings can be use to estimate several magnitudes by using current and position sensors signals as inputs to specifically designed state space observers. Magnitudes such as machining process forces and Tool Centre Point (TCP) acceleration, velocity and position can be estimated. More complex control strategies are going to be considered too, increasing computing power requirements.

This high computing power constraint, added to the other reasons explained bellow, has motivated the design of an advanced proprietary hardware.

Other design considerations.

Usually the machinery is made to fit the customer requirement, so the controller must be designed specifically for each machine. It must be taken into account that, in addition to the control of the spindle itself, it is necessary to manage or to control other subsystems integrated in the machine. Hence the hardware must be flexible enough to be adapted to a wide range of machine configurations.

Due to this variability it is important to consider the cost of the algorithms implementation process, which relies on both, processor flexibility and programming tools difficulty. The processor also defines the maximum computation power determining the limit of the control capabilities and complexity.

In the control tuning steps and in the machine start-up process as well as in the prototype development, a supervisory control is needed in order to monitory the behaviour and performance of the system. This is why the hardware design must consider real time data acquisition. This system allows monitoring and visualizing position data from sensors, machine subsystems states and even the value of internal variables used in the control algorithm.

CONTROL HARDWARE.

Even though the control hardware comes motivated by the magnetic spindle, its design remains valid to control a wide kind of industrial systems.

The hardware design consists in two boards, a digital board that manage processing tasks and an analogical board that serves as interface with the power electronics and with the machine subsystems. The platform has been designed in such an open way that it is possible to connect up to two digital boards and two interface ones, multiplying the computing power and interface flexibility of the design.

Digital board.
The digital board assembles three main processor elements. The following lines contain a brief description with most interesting features of each.

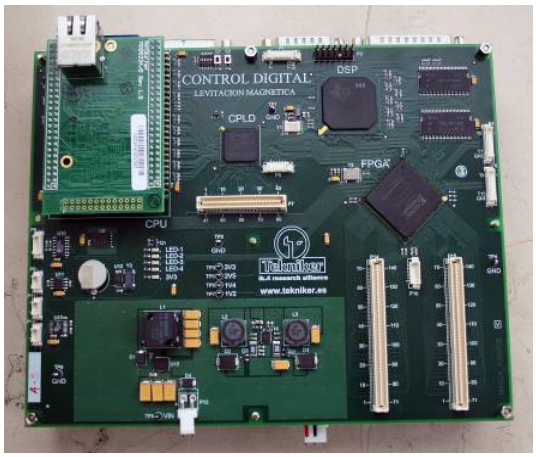

FIGURE 3: Digital board top view

FPGA SPARTAN 3. Spartan 3 FPGA is a high density device with 4000K logic gates that allows a complex hardware design implementation. It contains dedicated blocks to built RAM memory and 18 bits multipliers to optimize math operations performance. There are more than 400 user I/O pins. The I/O blocks can be configured to accommodate standard signal levels like TTL or CMOS, to facilitate the connection of external peripherals. This along with the concurrently task processing possibility, provides to a FPGA with a very high interface capability.

DSPTMS320C6713b. The DSP TMS3206713b is a floating-point processor from Texas Instruments with a 32-bit core which provides 1300 MFLOPS computing power at 300 MHz clock frequency. It performs a multiplication-add (MAC) floating point operation in one clock pulse and assemblies four floating point math coprocessor working in parallel in addition to fixed point coprocessor. There are a large number of peripherals: The Host Port Interface (HPI) allows external processor to access to the whole DSP memory map. The Direct Memory Access module (DMA) manages memory accesses without intervention of the CPU, transferring data from internal RAM to external memory devices through External Memory Interface port (EMIF). The DMA also manages HPI memory accesses.

NetBurner MOD5234. The NetBurner MOD5234 module is designed as a hardware Ethernet communication module. It has a Freescale Coldfire processor that implements the TCP/IP protocol. There is a considerable amount of both RAM and FLASH memory, available to storage data files, and an External Interface Module (EIM) for data transfer operations. Some standard communication port as RS232 and CAN Bus are implemented too.

Connection scheme of the processor elements. The three processors within the digital board are connected through some memory access ports and input/output pins.

The DSP has access via the EMIF to the FPGA‘s RAM and to its own external RAM. The Netburner module accesses to DSP memory map through HPI port and to the FPGA RAM through EIM. It also has an SD memory card connector and a 16 Mbytes Flash memory device as well as TCP/IP communication interface for an Ethernet network connection. The FPGA is connected by IRQ pins with the other two processors. It access to the board analog expansion bus where up to two analog boards can be connected. Due to the high connection lines density a CPLD is used to route this lines. The CPLD also is connected to de processor expansion bus, where another digital board can be connected.

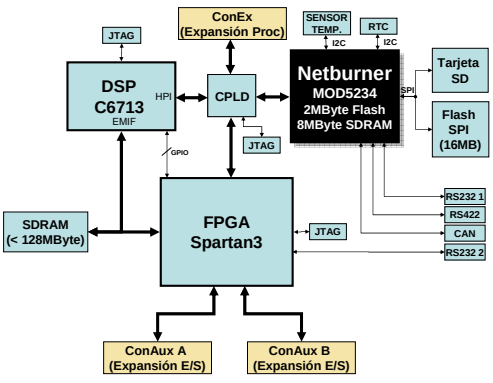

FIGURA 4: Processor connection diagram

Interface board.
This board groups all the system input and output channels and controls the interface with the remaining devices.

There are five fast analog inputs to manage position signals. These signals are filtered by eight pole antialiasing filters and then they are digitalized using 18 bits and 400Ksamples/s ADC.

Another twelve analogic inputs with a 16 bits and 250Ksamples/s ADC, six of them with four pole antialiasing filter, are available for general purpose use.

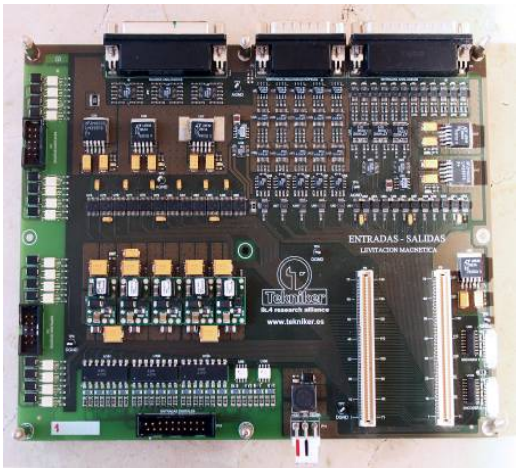

FIGURA 5: Interface board top view

Twelve analog outputs are implemented using 3Msamples/s DACs and a 175KHz signal reconstruction filters. Ten of these outputs are used as a reference input value for current amplifiers.

There are also sixteen digital outputs and the same number of digital inputs all of them optocoupled. They are being used as an enable signals connected to power amplifiers and to a refrigeration system, as a warning signals coming from temperature sensors or from Numeric Controller and as malfunction alarm signals.

Even thought they are not used in this application, there are two encoder inputs to control electric motors or linear drives.

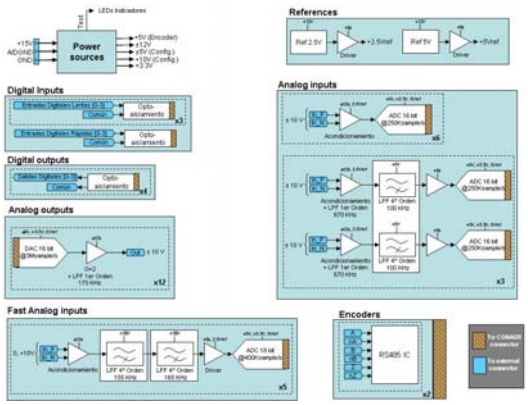

Fig. 6: Interface board resource diagram

The board has been designed in order to minimize the effect of the intra-board noise. This is important because of the great number of the resources that it includes.

CONTROL ALGORITHM DISTRIBUTION.

The control algorithm has been distributed among the three processor elements to maximize the computing capacity. Many of the tasks are performed concurrently, exploiting the specific capacities of each processor to perform those tasks for which they are more skilled. [4]

FPGA's algorithm.

The FPGA serves as an interface to access all the resources of the analogue board: encoders, digital inputs and outputs, analog input signals such as position sensors and temperature sensors signals and analogue outputs that control current amplifiers.

The signals are stored in RAM where they are accessible from the DSP. All accesses to the resources of the analog board are made in parallel way taking advantage of the FPGA ability to perform multiple tasks concurrently.

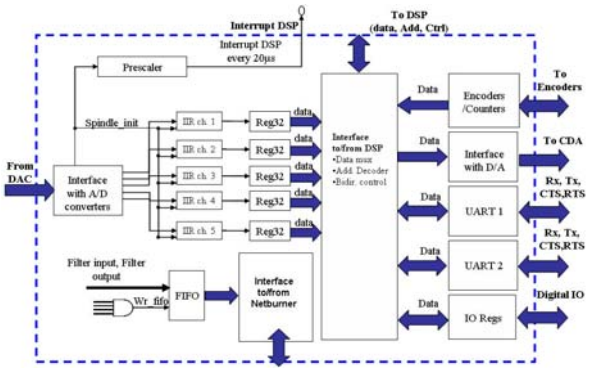

Fig. 7: FPGA algorithm block diagram

The position signals are filtered through lowpass IIR filters and stored in a FIFO for its acquisition by the NetBurner module. This data allow verifying the proper functioning of the filters. Type cast is applied to the filtered signal to convert in a floating-point variable and afterward is read by the DSP as a control input variable.

The FPGA also controls the control loop frequency. When it finishes input data acquisition triggers an interrupt pin and starts the control routine in the DSP.

DSP's algorithm.

The DSP performs the control task. This task begins when it receives the FPGA interruption signal through an IRQ pin. The DSP accesses to the position values in the FPGA RAM which are filtered using Kalman filters to remove noise. Then a PID control is applied to obtain the current values for power amplifiers, which are stored in RAM as data output. Both, the

writing and the reading memory access are made automatically by the DMA. Filtering and PID calculation are performed in floating point.

In addition to the control processing, the DSP performs monitoring task. In the idle task a state machine has been implemented which attends to warning signals and supervises the status of the machine subsystems. It also controls that the tool does not exceed the specified position limits and other potential failures such as clashes of the tool or overheating of the bearings coils. This task is performed in background so it does not interfere with the control task.

Simultaneously to the tasks described above, the real time acquisition data is made. The acquisition is done automatically by the DMA and practically it does not require CPU processing. Every control cycle, while the CPU performs the control calculations, the DMA transfers one data buffer from internal memory to external RAM. Once de acquisition ends the NetBurner module can access data through the HPI port and download it using TCP/IP connection.

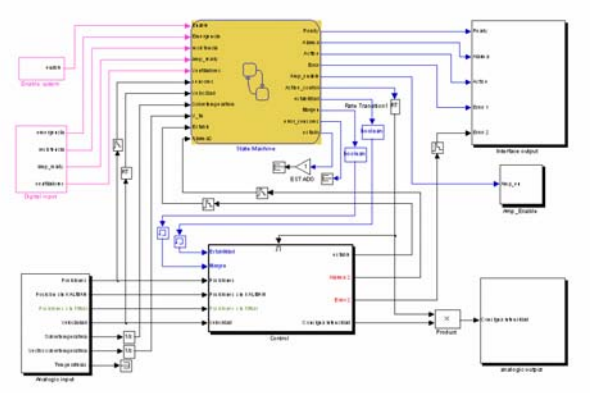

FIGURE 8: DSP control block diagram.

NetBurners algorithm.

The NetBurner module deals with the acquisition of real-time data and with downloading them through an Ethernet connection. The NetBurner is connected to the DSP through the HPI port. This port is managed by DMA peripheral in the DSP, so the NetBurner can access to the whole DSP memory map without interfering with its computing tasks. The NetBurner is also able to read and write the value of any variable defined in control algorithm such as filters coefficients, PID's coefficients, alarm flags… so it allows for comprehensive monitoring of system operation.

A communication protocol has been implemented to manage data exchange with a network connected PC. In this way, the PC can send variable read-write commands, on line configure data acquisition and download data via Ethernet.

The NetBurner also implements an FTP server from which data acquisitions and operating data files can be downloaded.

Monitoring and control PC program.

A graphical interface program has been developed on a Labview software development environment for visualising data acquisitions and as a system graphical control console. The software connects with the control board by TCP / IP and allows remote access to all control resources that has been detailed in the preceding paragraphs.

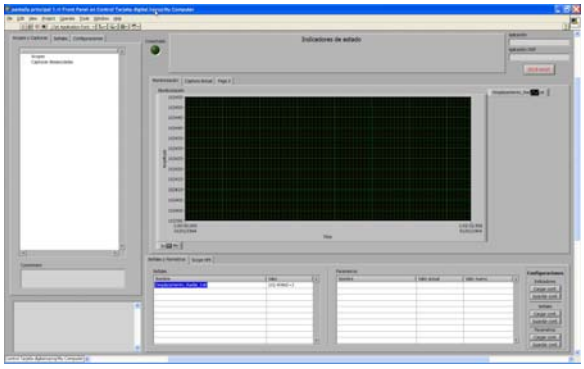

Fig. 9: Graphical interface PC program

The Graphical interface PC program is directly connected to the NetBurner module and it implements the same data exchange protocol. The PC program acts as a master in the data exchange and it decides which data is accessed and when the data acquisition starts.

BOARD PERFORMANCE AND BENEFITS.

To measure the electronic board performance several tests have been done.

A speed comparison between the new hardware and a high performance National Instruments Control Board NI-PXI-8106RT was done. While National Instrument Board is able to perform one floating point PID at 94 KHz frequency, the control hardware here presented performs five channels of PID plus four pole IIR filter at 250 KHz. This suppose at least 10 times faster, even if not considering the IIR filter calculation.

The performance of the implemented control algorithm has been measured and is explained below.

The control loop frequency is 50 kHz, i.e. 20 μs period. The control routine takes 15 μs to calculate the current output values leaving 5 μs to the idle task to process the state machine and the monitoring task.

At the same time the control variables read/write accesses are performed and, if it has been configured, the acquisition of real time data. The DMA transfers 10 words (40 bytes) every memory access taking three or four μs.

The real-time data acquisition allows a maximum of 10 variables simultaneously. It can choose any variable defined in the control routine. The DSP external RAM has 64 Mbytes for data storage, which represents more than 6 Mpoints per variable.

The graphical interface program lets user set up and view the data acquisitions, change the value of any variable in memory and access all of the control electronics resources. It also incorporates all the necessary elements to manage the operation of magnetic spindle behaving as a control console for the magnetic bearings system. The communication is done via the TCP / IP protocol so that all operations can be performed remotely.

Fig. 10: Magnetic spindle prototype

The control electronic is being tested in a newly built magnetic spindle in Tekniker-IK4 facilities.

FUTURE WORKS.

The control electronics is one of the projects that the Magnetism group, in collaboration with the Electronics department, is developing for magnetic spindles application. Other related projects are the design of power electronics that supplies the bearing windings and the implementation of position sensors. To meet these new developments a PWM module in the FPGA to directly control the switching power devices and new modules for position signal acquisition are planned to implement.

On the other hand automatic programming tools are being tested. Embedded Target for TI C6000 DSP from Matlab/Simulink eases the work with the DSP. This utility, along with the Simulink Real-Time Workshop, allows obtaining C language models from designs already made with Simulink blocks. AccelDSP from Xilinx is other specific software that allows automatic translation of a design from Matlab environment to a device specific VHDL. This software was in fact used to implement filters on the FPGA.

The computing power of the control electronics allows to implement complex control strategies to improve the system performance. As it has been said before a specific state observer for special machining parameters are in development and more complex non linear control strategies are being taken into account.

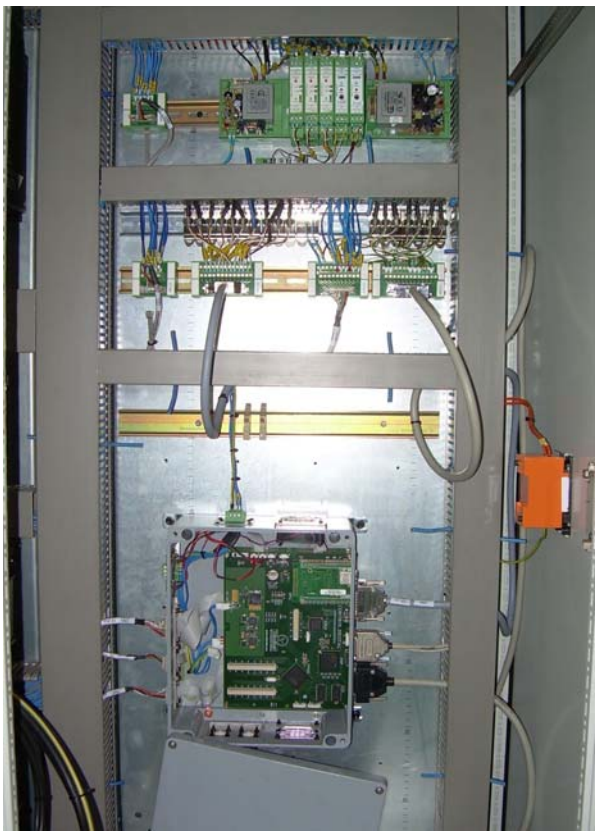

Fig. 11: Control electronics mounted in an electric cabinet

REFERENCES

[1] Active Magnetic Bearings. Basics, properties and applications of active magnetic bearings. Gerhard Schweitzer, Hannes Bleuler, Alfons Traxler. ISBN 3 7281 2132 0

[2] "Motor spindles – Latest state of technology" Gebert, K. (WEISS GmbH). STC M, 57th CIRP General Assembly 2007, Dresde (Germany).

[3] "Magnetic bearings and machine tools applications" Lacour, M. (S2M company). STC M, CIRP January meetings 2005, Paris (France).

[4] "Migration from Control Algorithms Described in Matlab/Simulink to FPGA-DSP Based Platform" Jon Mabe, José Antonio de Alayo, Itziar Marín, Alberto Izpizua, Aitzol Zuloaga. 3rd FPGAworld Conference, November 2006, Stockholm (Sweden) ISSN 1404-3041 ISRN MDH-MRTC-204/2006-1-SE I